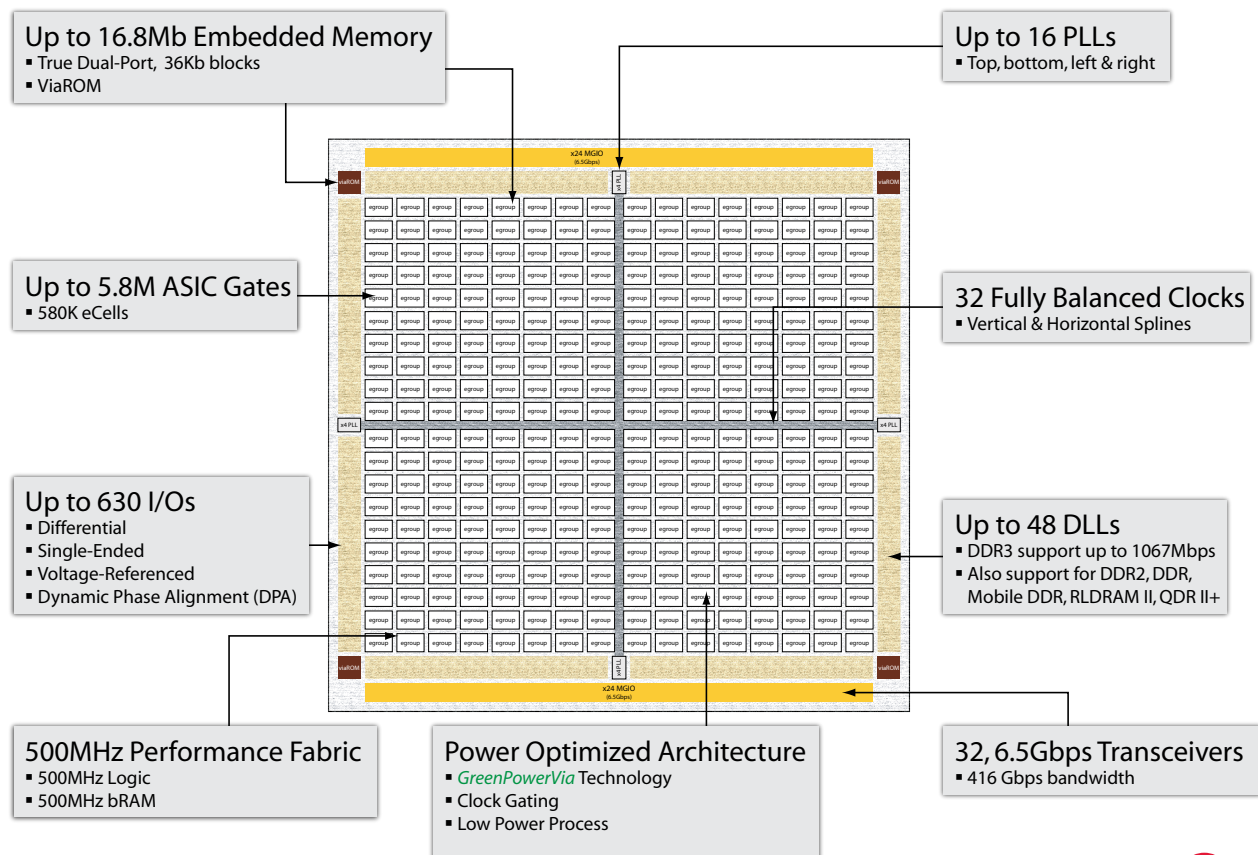


45nm NEW ASIC with 6.5Gbps Transceivers, Affordable for All

eASIC Nextreme-2T Overview

eASIC Nextreme-2T is a family of NEW ASIC devices, manufactured on a 45nm CMOS process, and built using eASIC's patented single-via customization technology. The eASIC Nextreme-2T family provides ASIC-like performance, power and low unit-cost, combined with a FPGA-like design flow and rapid delivery of devices. eASIC Nextreme-2T is built on a breakthrough configurable fabric which combines an efficient Look-Up-Table (LUT) based logic with a single via-layer customized interconnect. eASIC Nextreme-2T delivers many enhancements and advantages for designers considering standard cell ASICs, FPGAs and ASSPs.

The eASIC Nextreme-2T family features up to 580K logic elements (eCells) with up to 32 full duplex high speed SERDES (MGIO) operating up to 6.5Gbps.



Cost Advantage

A simple, area efficient, single Via routing scheme, enables eASIC Nextreme-2T devices to be manufactured within a much smaller die area than equivalent density SRAM FPGAs, thereby reducing device cost. In addition, as only one layer needs to be programmed for each customer design, the up-front development cost, time and risk is significantly lower than that of cell-based ASIC.

Power Advantage

Use eASIC Nextreme-2T to reduce power consumption by up to 80% compared to FPGAs:

- Static Power Reduction Techniques**
 Low static power through use of 45nm Low Power (LP) CMOS process, triple-oxide transistors and eASIC's patented *GreenPowerVia* technology. *GreenPowerVia* powers off all unused eCells, bRAMs, and Register Files.
- Dynamic Power Reduction Techniques**
 Techniques such as multiple core voltage options (down to 1.0V), clock gating and via-based interconnect also help to minimize dynamic power.

Low Power 6.5Gbps MGIOs

eASIC Nextreme-2T is designed to support the widest possible range of protocol standards across multiple data rates, while offering excellent signal integrity and achieving the lowest power consumption. A 6.144Gbps Common Packet Radio Interface (CPRI) compliant eye diagram is shown adjacent.

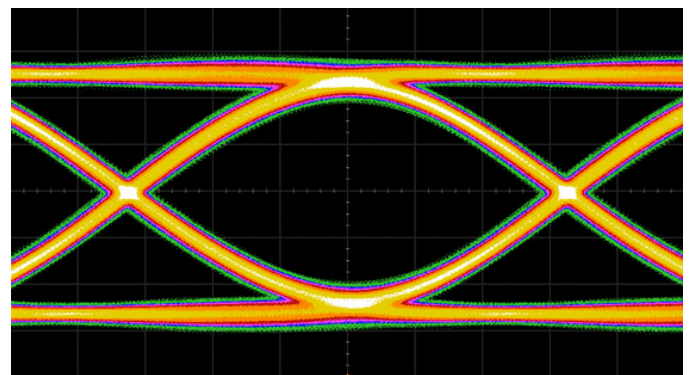
Get Started

To learn more on how you can replace your expensive, power hungry FPGAs or your legacy ASICs visit www.easic.com or contact your local eASIC representative.

eASIC Nextreme-2T Family

	N2XT330	N2XT580
eCells	331,776	580,608
Equivalent Gates (Millions)	3.9	5.9
ViaROM (# of blocks)	4	4
ViaROM (Kbits)	1,024	1,024
bRAM (# of blocks)	288	468
bRAM (Kbits)	10,368	16,848
PLLs	16	16
DLLs	48	48
MGIO 6.5 Gbps Transceivers	24	32
Packages and User IO		
FC780 (29x29)	16 / 400	16 / 400
FC1152 (35x35)	8 / 630	8 / 630
FC1152 (35x35)	24 / 556	24 / 556
FC1152 (35x35)		32 / 480

CPRI 6.144Gbps Eye Diagram



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