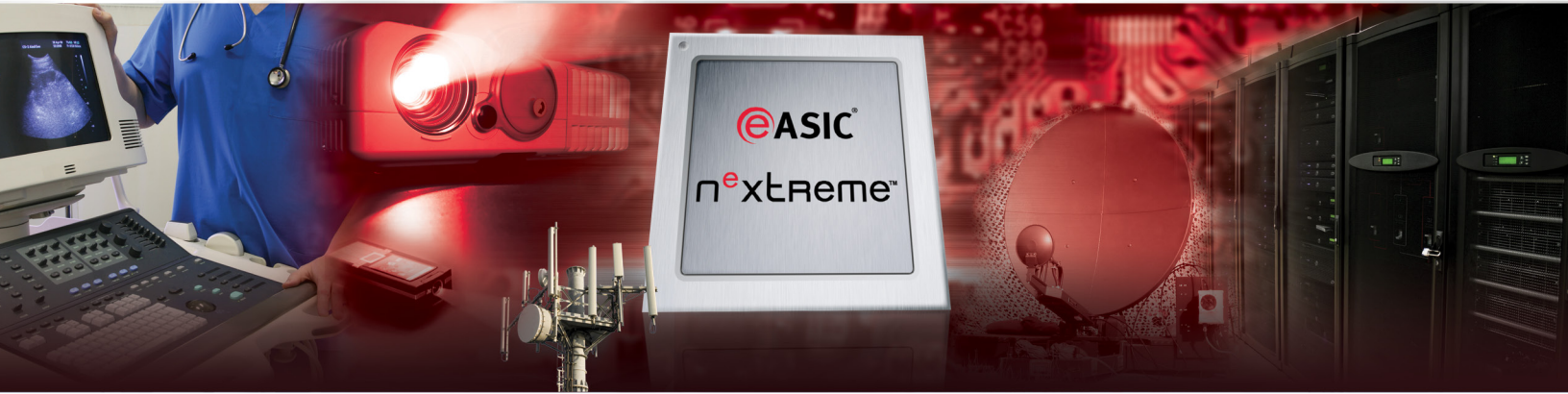
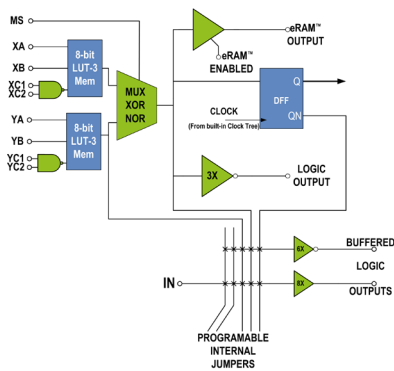


eASIC n^exTreme™ 90nm NEW ASICs



eASIC Nextreme - 90nm NEW ASIC

eASIC Nextreme is a family of NEW ASIC devices, manufactured on a 90nm CMOS process, using eASIC's patented customization technology. They are built using a breakthrough patented configurable logic technology, which combines an FPGA-like logic cell, called an eCell (below), with single via customizable routing. This technology enables eASIC Nextreme devices to provide you with compelling low cost-of-ownership both for fast prototyping and high volume production.



The Figure adjacent shows a benefits comparison between FPGAs, Cell-based ASICs and eASIC Nextreme devices. The programmable nature of SRAM-based FPGAs comes with severe cost and power penalties as each programming interconnect requires transistors and SRAM cells that consume both real-estate and power consumption. Through utilizing patented, single via customizable routing, instead of twenty-five year old FPGA-based programmable interconnect routing, eASIC Nextreme delivers unit-cost and power consumption that approach Cell-based ASICs thereby relaxing the constraints on your system design.

Another unique advantage of eASIC Nextreme's via customizable routing method is the requirement of only a single via layer (via 6). This via layer can be implemented using Direct-write e-Beam (electron beam) and therefore significantly reduces mask costs and hence risk.

eASIC Nextreme allow designers to implement sophisticated IP cores such as Tensilica Diamond Standard Processors and DDR2 memory controllers to help you to get to market quickly. You need no longer be locked into an FPGA vendor's limited proprietary IP cores.

	SRAM FPGA	Cell-based ASIC	eASIC Nextreme NEW ASIC
Power Consumption	Highest	Lowest	Low
Unit Cost	Highest	Lowest	Low
Up-front Development Cost	Low	High	Low
Design Flow	Simple	Difficult	Simple
Fast Turnaround	Yes	No	Yes
Instant On	No	Yes	Yes

Once you hand off your design to eASIC, the 90nm NEW ASIC prototypes can be delivered in 5 weeks instead of months as with traditional Cell-based ASICs. You can use these prototypes to demonstrate working solutions to your customers or go into mass production, as the prototyping and production devices are identical.

With eASIC Nextreme you truly get the best of both worlds i.e. unit cost and power consumption approaching that of a cell-based ASIC, coupled with low up-front development costs and fast turnaround as with FPGAs.

eASIC Nextreme NEW ASIC Device Family

eASIC Nextreme Family Details

Member	Equivalent Gates	eCells	Distributed RAM (Max.)		Block RAM		PLLs	DLLs
			eRAM Blocks	eRAM Bits	bRAM Blocks	bRAM Bits		
NX750LP	350,000	26,624	104	416K	13	416K	4	6
NX750	750,000	55,296	216	864K	27	864K	6	8
NX1500	1,500,000	100,352	392	1568K	49	1568K	8	8
NX2500	2,500,000	169,984	664	2656K	83	2656K	10	12
NX4000	4,000,000	276,480	1080	4320K	135	4320K	10	16
NX5000	5,000,000	358,400	1400	5600K	175	5600K	10	20

eASIC Nextreme Package Options and User I/Os

Package (mm)	128-pin TQFP (14x14)	208-pin BTBGA (15x15)	233-pin BTBGA (10x10)	324-pin BTBGA (19x19)	480-pin PBGA (23x23)	480-pin FCBGA (23x23)	672-pin PBGA (27x27)	672-pin FCBGA (27x27)	896-pin PBGA (31x31)	896-pin FCBGA (31x31)	1152-pin FCBGA (35x35)
NX750LP	68	144	146	232							
NX750			146	232	298						
NX1500					298	323		438			
NX2500					298	298	451	448	506	570	
NX4000							438		569	617	730
NX5000										617	790

- Notes:
- Each eCell contains two 3-input Look Up Tables and a Register.
 - eRAM is a configurable, distributed, dual-port memory flexibly traded off with logic cells.
 - "K" = 1,024.

Get Started

To learn more visit www.easic.com or contact your local eASIC representative.

TRADEMARK INFORMATION

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