



SEAMLESS MIGRATION FROM eASIC NEXTREME/NEXTREME-2 TO CELL-BASED ASIC

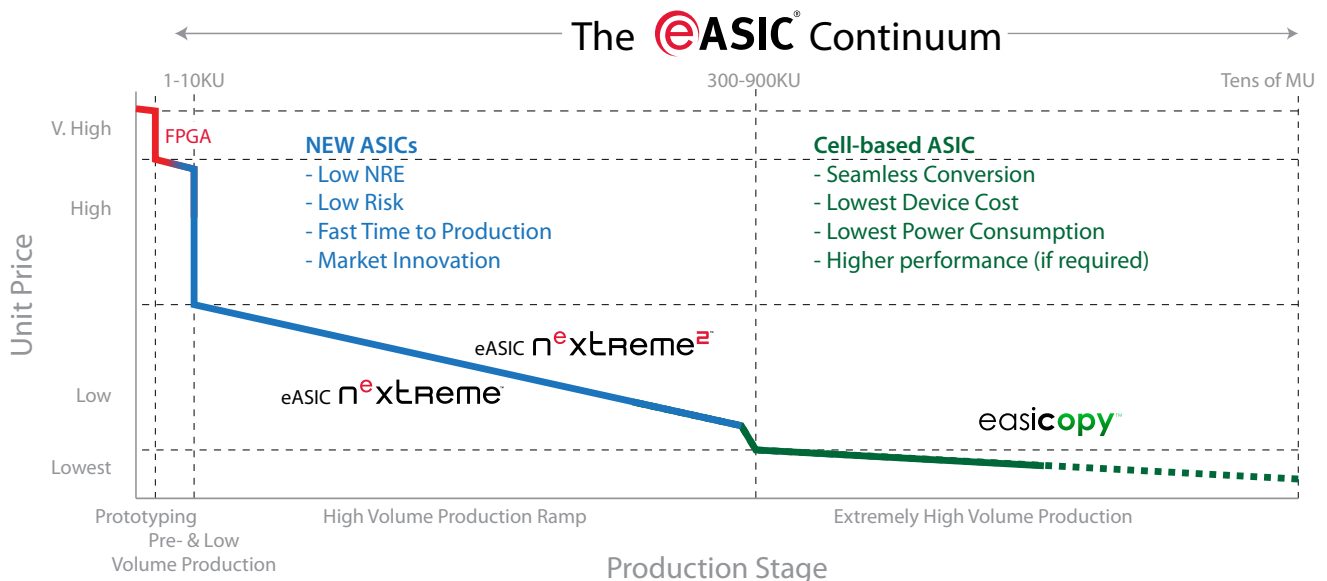
easicopy™ Overview

easicopy™ ASIC provides OEMs with a low risk, cost reduction path to cell-based ASIC and hence even higher gross margins. OEMs have peace of mind that as their product succeeds in the market, they have a solid path to cost reduction, and many see easicopy ASIC as a vital addition to their existing value engineering programs.

The eASIC Continuum

With eASIC as a partner, OEMs have multiple solutions for cost reduction that can provide the optimum choice for their product evolution:

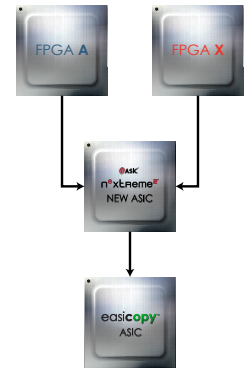
- During market exploration or early volume ramp, greater market uncertainty may exist that may make it difficult to justify a cell-based ASIC NRE. eASIC's low up-front NRE eASIC Nextreme or Nextreme-2 NEW ASIC devices enable OEMs to minimize risk while bringing profitable products to market early, and secure early customer design wins.
- When initial customer successes transition to very high volume production, easicopy ASICs provide OEMs the choice to further reduce cost, power consumption and increase performance via a cell-based ASIC migration.



FPGA Agnostic

Through partnering with eASIC, OEMs have the flexibility of an FPGA agnostic cost reduction path. FPGAs from Vendor-A or Vendor-X can be chosen based on their technical merits such as features, performance, power consumption or design tools.

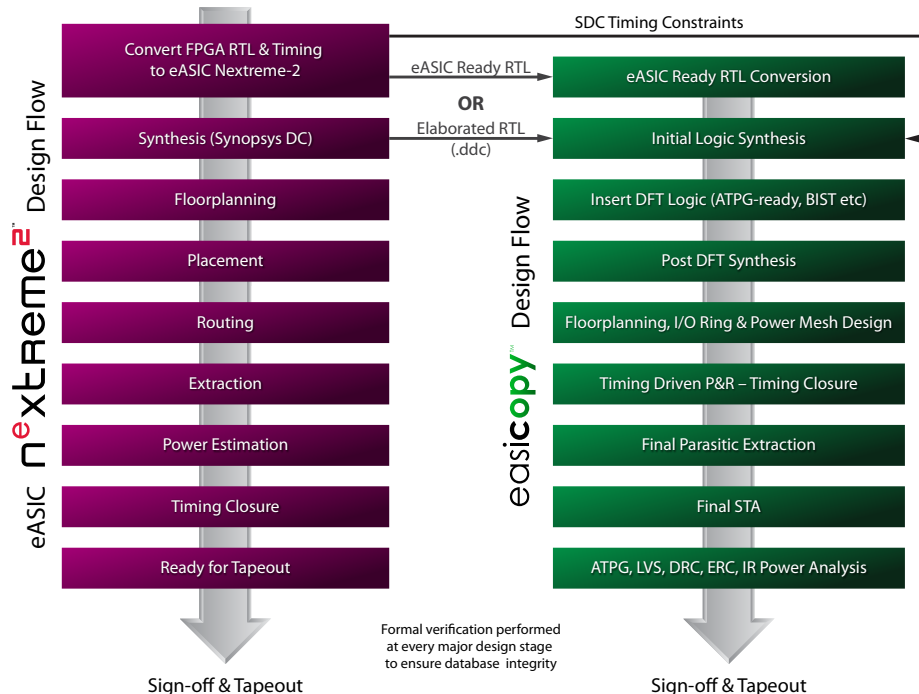
Once the FPGA design is stable, the OEM works with eASIC to cost (or power) reduce their design to a single via-programmable eASIC Nextreme or Nextreme-2 NEW ASIC device. eASIC engineers have successfully performed many FPGA conversions to eASIC Nextreme or Nextreme-2 devices which are now in production in applications ranging from consumer devices to carrier class wireless infrastructure equipment.



FPGA Agnostic Cost Reduction

Proven Design Flow

The easicopy design flow is shown below. At the front end it requires a eASIC Nextreme or Nextreme-2 synthesized netlist and an SDC timing constraints file. After initial synthesis, the design is taken through a traditional cell-based ASIC flow by eASIC engineers. This includes Design For Test (DFT) insertion and synthesis, and then back-end physical implementation which includes floorplanning, I/O ring design, power mesh design, timing driven place and route, timing closure, parasitic extraction, final STA, and tapeout readiness. eASIC engineers have extensive experience in converting FPGA designs to via-programmable eASIC Nextreme or Nextreme-2 NEW ASIC, and then eASIC Nextreme or Nextreme-2 NEW ASIC designs to cell-based, easicopy ASIC.



Get Started

To learn more on easicopy™ ASIC visit www.easic.com or contact your local eASIC representative.

www.eASIC.com

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eASIC Corporation

2585 Augustine Drive,
Suite 100,
Santa Clara, CA 95054, USA

Tel: 408-855-9200
Fax: 408-855-9201

info@eASIC.com
www.eASIC.com